FAIRCHILD
SEMICONDUCTOR®

AN7935
EVALUATION BOARD
APPLICATION NOTE

FEATURES

- 12-Bit Resolution
- Up to 20 MSPS Conversion Rate
- Single +3.3 V Supply Required for SPT7935
- On-Board Clock Driver
- On-Board Adjustable References and Common Mode
- On-Board Single-Ended to Differential Input Buffers With Adjustable Level
- On-Board Single-Ended to Differential Transformer (1:1)
- Digital Output Buffer
- +3.3/5 V Logic Output

APPLICATIONS

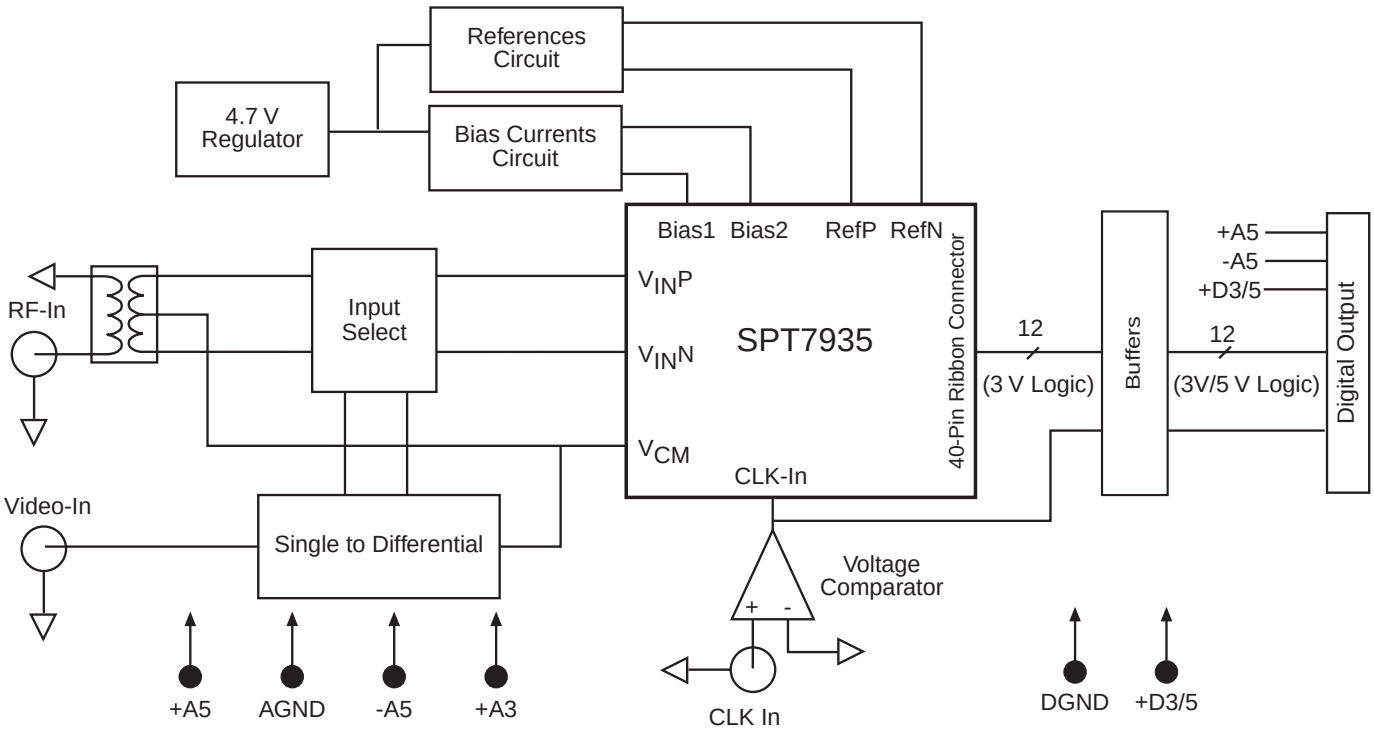
- For Low Power, High-Speed Design Applications
- Evaluation of the SPT7935
- Engineering System Prototype Aid
- Major Block for Prototype System
- Guide to System Layout
- AC Dynamic Analysis of the SPT7935 (With Customer-Provided Data Capture and FFT System)

GENERAL DESCRIPTION

The SPT7935 is a 12-bit, 20 MSPS ADC (analog-to-digital converter). It is a fast differential analog input device that provides outstanding dynamic performance with very low power dissipation and operates with a +3.3 V supply. It is provided in a 44-lead Thin Quad Flat Pack (TQFP) package. The EB7935 evaluation board is intended to be used as a tool for device characterization and to demonstrate the performance of the SPT7935 ADC.

The AN7935, application note for the EB7935, has ten separate sections: Power Supplies and Grounding, Layout, Reference Circuits, Bias Circuits, Analog Inputs, Common Mode Voltage, Clock Circuit, Digital Output, Control Options and Test Points, and Setup and Calibration. Figure 6 is a detailed schematic of the evaluation board. Table III lists the materials and parts for the EB7935. Layouts of the board layers are included (figures 7, 8, 9 and 10).

BLOCK DIAGRAM



The SPT7935, monolithic 12-bit ADC, can sample the input at a rate up to 20 MSPS. Its logic inputs and outputs are compatible with +3.3 V logic. The analog input of the SPT7935 permits ±1 V differential (typical) with +1.5 V of common mode voltage, internally provided. The board supports straight AC transformer coupling of the input signal or op-amp buffering as a single-to-differential converter. Both signals are exclusively input. The 12 digital output bits and the sample clock are buffered out for downstream digital processing.

The EB7935 features on-board voltage references that allow the user to adjust the top and bottom of the reference ladder as well as the bias current.

The clock comparator/buffer allows sine wave input to generate the TTL sample clock. This also allows for a modest variation of the sample clock duty cycle.

Four separate voltage inputs power the various circuits on the evaluation board. They are: +5 V analog, -5 V analog, +3.3 V analog for the SPT7935 (which also powers the +3.3 V for SPT7935 digital outputs via a ferrite bead) and an adjustable +3/5 V digital output for the output buffers. The board has room on either side for breadboarding of additional circuits as required by the user. Fairchild suggests you use the left side prototype area for analog and the right side for digital circuits.

POWER SUPPLIES AND GROUNDING

The EB7935 requires analog +5 V and - 5 V (designated +A5 and -A5 on the board), digital +3.3 or +5 V for output (designated +D3/5 on the board), and a +3.3 V analog supply for SPT7935 operation (designated +A3 on the board).

The +A5 and -A5 supply the input buffer operational amplifiers, reference circuits, clock generator comparator and reference generation device (+4.7 V reference). The +D3/5 digital supply provides for two logic levels on the digital output. The +A3 supplies the internal circuit operation of the SPT7935.

Power supply connection points are labeled for operator convenience. Before connecting any power supply to the evaluation board, set the supply to the correct value and power off. Ensure that all power supplies are connected and preset before full power is applied. Figure 1 shows the proper connection of the power supplies. After power-up, verify that the supply voltages are within specification before proceeding. (Refer to table I.) Make any necessary adjustments, referencing your measuring instrument to the appropriate return node.

Figure 1 - Power Supply Connections

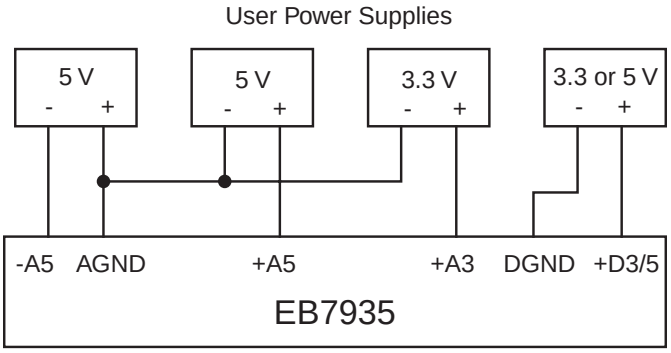


Table I - Power Supply Specifications

	V_{MIN}	V_{TYP}	V_{MAX}	I_{TYP}
-A5	-4.9 V	-5 V	-6 V	-54 mA
+A5	+4.9 V	+5 V	+6 V	+60 mA
+A3	+2.7 V	+3.3 V	+3.6 V	+22 mA
+D3/5	+2.7 V	+5 V	+5.5 V	+26 mA

The SPT7935 design uses a common analog and digital ground plane. The EB7935 application board separates the analog and digital grounds at the final digital buffer drivers U9 - U10. Fairchild recommends connecting analog and digital grounds together with a ferrite bead at this split.

LAYOUT

This evaluation board has four layers: two signal layers (top and bottom layers), one ground plane layer (both analog and digital) and one power layer that accommodates all power distribution including all post-power supply filtered power. The ordering of the layers is as follows: the top is the signal layer (used for critical signals requiring controlled impedance), the second is ground, third is power and bottom is signal. The signal layers are designed with a controlled characteristic impedance of 50 ohms. Figures 7, 8, 9 and 10 show the actual layout for the EB7935.

REFERENCE CIRCUITS

The common on-board reference voltage is established from a TK11247B (+4.7 V reference, low drop out). This reference voltage is used to set the SPT7935's reference ladder voltages via U3 with the adjustments of potentiometers R1 and R2. Nominal voltage for the reference is +1 V (low reference, V_{REF}-) and +2 V (high reference, V_{REF}+). Adjust R1 and monitor the V_{RN} test point to set the V_{REF}-. Adjust R2 and monitor the V_{RP} test point to set the V_{REF}+. This evaluation board is designed to limit the reference voltages so as not to exceed specifications during normal operation.

The range for V_{REF}+ is from +1.5 to +2.5 V, and the range for V_{REF}- is from +0.5 to +1.5 V on this evaluation board. The recommended minimum delta between V_{REF}+ and V_{REF}- is 0.6 V, with the maximum delta of 1.6 V.

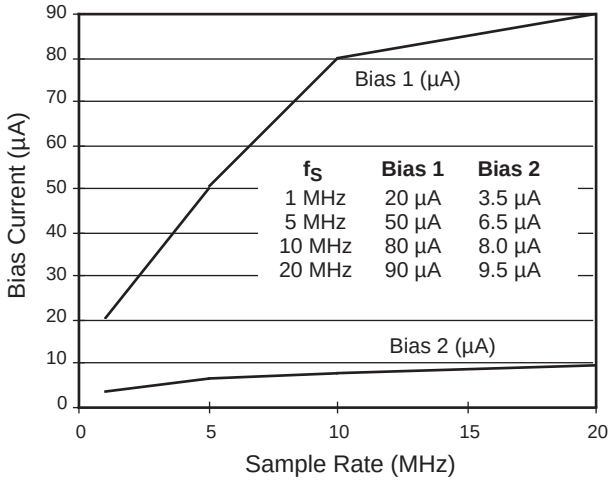
The analog input full scale voltage range (FSR) is a function of the delta voltage between the V_{REF}+ and V_{REF}-.

Note that U3, an OP291, is supplied only from a +5 V supply. This technique is used to ensure that the reference ladder never goes negative at power up and that the reference voltage potentials are always positive.

BIAS CIRCUITS

The best AC performance is achieved when the bias currents are optimized for the selected sample rate. Figure 2 shows the settings for Bias 1 and Bias 2 at selected frequencies.

Figure 2 - Suggested Bias Currents vs Sample Rate



It is critical to measure the bias voltage across the specified resistor and not at the bias pin on the device since the bias voltage changes as the bias current changes. Figures 3 and 4 show the relationship between the bias current and the bias voltage.

Adjust the current for Bias 1 by measuring the voltage drop across R17 using test points B1P and B1N. Calculate the current, using the measured voltage and the specified resistance. Adjust as necessary.

Adjust the current for Bias 2 by measuring the voltage drop across R16 using test points B2P and B2N. Calculate the current, using the measured voltage and the specified resistance. Adjust as necessary.

Figure 3 - Bias 1 Voltage vs Bias 1 Current

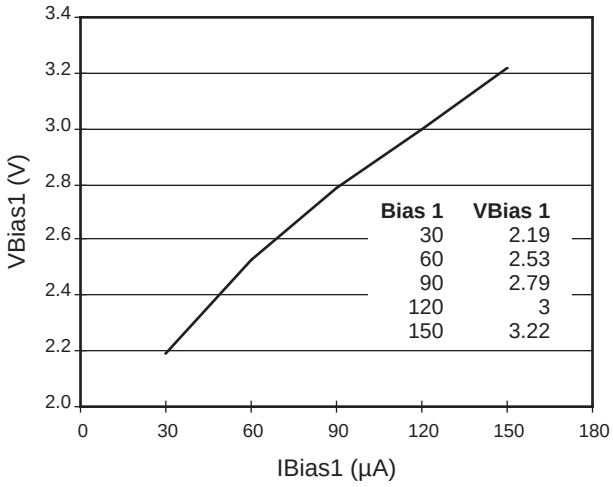
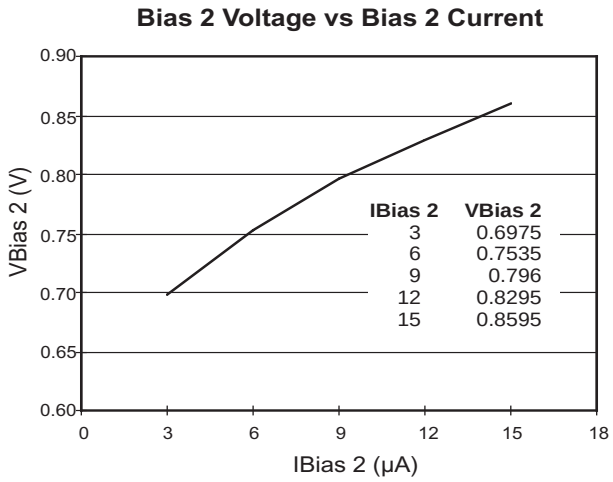


Figure 4 - Bias 2 Voltage vs Bias 2 Current



ANALOG INPUTS

Analog input signals required for the SPT7935 are differential video input signals presented to the V_{IN}+ and V_{IN}- pins.

The differential video input signals may be applied from either one of two input circuits. The first is a single-ended to differential RF transformer, and the second is through an op-amp circuit that takes a single-ended input and creates a differential analog input signal for the SPT7935.

The transformer circuit consists of a mini-circuit T1-6T RF transformer (1:1, with center tap), center-tapped secondary with a 1 dB passband from approximately 50 kHz to 300 MHz. In this design, the differential output is loaded to a 50 ohm load, reflecting this back to the primary for impedance matching and maximum power transfer. In addition, there is a 180 degree phase inversion from the input at the RF-In to the differential input to the SP7935. Ensure that J1 and J2 are jumpered appropriately when using the transformer input as the signal source.

The center tap of the RF transformer is driven by the V_{CM} output pin of the SPT7935. V_{CM} is typically one-half of V_{DD}, which translates to 1.5 V nominal on the EB7935. The maximum input signal allowed at RF-In is 2 V peak-to-peak.

The Video-In signal source is processed by two op-amps (OPA642, U6 and U7) to create the differential input signal. The offset voltage required for the common mode is generated by U5 (OP191). The operation of the two operational amplifiers is as follows.

Selection criteria of buffer op-amps are as follows:

- Dynamic Range (open loop gain of >75 dB)
- Gain Bandwidth >50 MHz
- THD < 75 dB
- SNR > 75 dB

The V_{IN}+ buffer operates as follows. The Video-In signal is applied through an BNC connector terminated to 50 ohms Thevenin equivalent. The common mode voltage biases the level of the inverting input to maintain CM. The input is resistor divided by two and applied to the noninverting input. The amplifier is designed to produce a gain of two. The results of this inputs a signal that is of the same amplitude and in phase with the single-ended input signal.

The V_{IN}- buffer operates as follows. The Video-In signal is applied through an BNC connector terminated to 50 ohms Thevenin equivalent. The common mode voltage is summed into the inverting input of U7, while the noninverting input is referenced to analog ground, with the input and feedback resistors the same. The result of the output is the algebraic sum of the input voltages (V_{IN} and Common Mode). The common mode voltage sets the mid-scale value. The results of this amplifier signal are of the same amplitude and out-of-phase with the single-ended input signal.

The output of the amplifiers directly feeds the input of its respective side. In addition, clamping diodes (D1-4, SB101B) are designed in to ensure that the input levels at power up and during any other anomalistic occurrence do not exceed the limit specification for the input to this device. A monitoring test point is designed into the PCB for direct observation of the signals into the SPT7935.

Fairchild recommends appropriate bandpass filters on the input when performing AC characterization of this part.

COMMON MODE VOLTAGE CIRCUIT

The SPT7935 has an on-board common mode voltage reference. It is typically one-half of V_{DD} and is capable of driving up to 20 μA. It is used for either one of two purposes on the EB7935. One use is to drive the center tap of the RF transformer at the RF-In connection. The second use is to provide level shifting for the single-to-differential converter present at the Video-In connection.

CLOCK CIRCUIT

Fairchild recommends a 50% clock duty cycle, ±3%. On-board clock drive is performed by a TTL comparator. The comparator's reference is set by a variable DC voltage input to the inverting input. The drive signal is assumed to be a sinusoid signal; however, any modified signal with correct clock pulse width high and low is allowed. The compare level is between ±1 V. When using a sinusoid input, be sure not to allow the compare level to reach the crest of the signal as this may cause serious jitter problems at the output of the comparator. (A slow slew rate will cause this with any comparator.) However, the drive signal is capable of exceeding these comparator levels, up to a maximum value of ±2.5 V.

The output of the TTL comparator goes to a 74LVX00 NAND gate. This device acts as a level translator accepting the TTL (0 to 5 V) levels from the output of the comparator and producing the 0 to +3.3 V drive levels for the SPT7935.

Ensure the clock source signal is capable of driving a 50 ohm load. If not, remove or modify the input termination resistor (R36) to accommodate the user's drive circuit.

DIGITAL OUTPUT

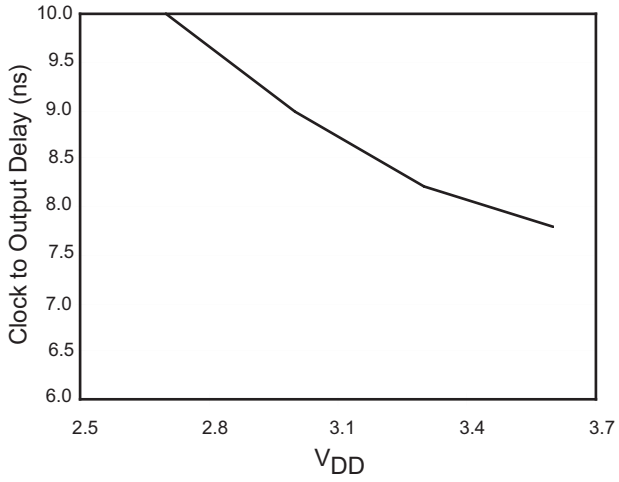
The SPT7935 output is a 3.3 V logic level. Voltage translator ICs were used to accept this logic level and support either +3.3 or +5 V logic levels on the output. To accommodate either output, adjust the +3.3/5 V power supply. Digital buffers U9 and U10 on the EB7935 can operate at either voltage. Refer to figure 6 for the J1 connector pinout.

Data buffers are furnished with the EB7935. The user will furnish required latch and/or data storage circuitry external to the EB7935.

Note that series damping resistors (value of 51 ohms) are in series with the output of the SP7935 and J1 outputs to reduce oscillation when there would be a mismatch of impedance, long signal or cable lengths from the output of the EB7935 to the user's receiver circuit. These may be modified or replaced with zero ohm resistors as the user's application requires.

The clock to output delay is typically 9 ns. This parameter will changes as a function of V_{DD}. Figure 5 shows this relationship.

Figure 5 - Clock to Output Delay vs V_{DD}



CONTROL OPTIONS AND TEST POINTS

Table II outlines the names, use and intent of the jumpers, test points and control potentiometers.

Table II - Jumper Descriptions

Name	Description	Intended Use
R1	Potentiometer	Adjust the V_{REF}- value. (Range between +0.5 and +1.5.)
R2	Potentiometer	Adjust the V_{REF}+ value. (Range between +1.5 and +2.5.)
R3	Potentiometer	Adjust the threshold for the clock comparator. (Range from + to - 1 V.)
R4	Potentiometer	Adjust the Bias 1 input current (typical value of 90 ma, for 20 MSPS). Measured voltage across R17 (4.75 kΩ) will determine the current.
R5	Potentiometer	Adjust the Bias 2 input current (typical value of 9.5 ma, for 20 MSPS). Measured voltage across R16 (100 kΩ) will determine the current.
+R4.7	Test Point	Measure the regulated +4.7 V reference device.
Vrp	Test Point	Measure the voltage high reference input to the DUT.
Vrn	Test Point	Measure the voltage low reference input to the DUT.
B1p/b1n	Test Points	Used together to measure the voltage across the resistor feeding the Bias 1 current input. Used to determine the input current.
B2p/b2n	Test Points	Used together to measure the voltage across the resistor feeding the Bias 2 current input. Used to determine the input current.
+CM	Test Point	Used to measure the common mode voltage that is sourced from the common mode output of the DUT.
-CM	Test Point	Used to measure the offset voltage (common mode) that will be applied to the dual op-amp buffers to create the differential input to the DUT.
VP (PTP2)	Test Point	Oscilloscope probe test point with short ground connection to accurately measure the positive input signal.
VN (PTP3)	Test Point	Oscilloscope probe test point with short ground connection to accurately measure the negative input signal.
J1	Jumper Pins	Allows selection of the transformer (inverted input) or buffered analog input signal to V_{IN}+.
J2	Jumper Pins	Allows selection of the transformer (inverted input) or buffered analog input signal to V_{IN}+.

SETUP AND CALIBRATION

The setup and calibration operation involves setting power supplies, connecting and powering-up, establishing the desired reference voltages, setting Bias 1 and Bias 2, setting up and verifying sample clock operation and verifying functional operation of the output of the EB7935. The following setup assumes video input is used for test.

1) Power supplies: Disconnect the power supplies from the EB7935. Set power supplies per table I. Turn off the supplies and connect the power supplies to the evaluation board. Turn on all power supplies simultaneously.

2) Reference: Adjust R1 while monitoring the V_{RP} test point and set it to +2 ±0.005 V. Adjust R2 while monitoring the V_{RN} test point and set it to +1 ±0.005 V. Adjust Bias 1 (potentiometer R4) to produce a voltage reading across B1P and B1N to 0.427 ±0.001 V. Adjust Bias 2 (potentiometer R5) to produce a voltage reading across B2P and B2N to 0.95 ±0.001 V.

3) Sample Clock: Set the user-provided TTL or sine wave clock. Ensure that the clock frequency and duty cycle are within the part's specification. Connect the clock to the CLK IN, BNC connector on the evaluation board.

4) Analog Input: Set up a 1 V_{P-P}, symmetrical around ground, 1 MHz sine wave signal. Connect this signal to Video-In. Jumper J1 and J2 to section B.

5) Digital Output: If you don't have a digital capture system for processing and observing data, use an oscilloscope or logic analyzer to observe the digital encoded data of the analog input signal. Another option is to purchase the EB9713 board (the board features the SPT9713, a 100 MWPS TTL DAC) that mates up easily with the EB7935. This board may be used for reconstruction of the encoded data for spectral analysis.

Figure 6 - Detailed Schematic, Rev. B Board

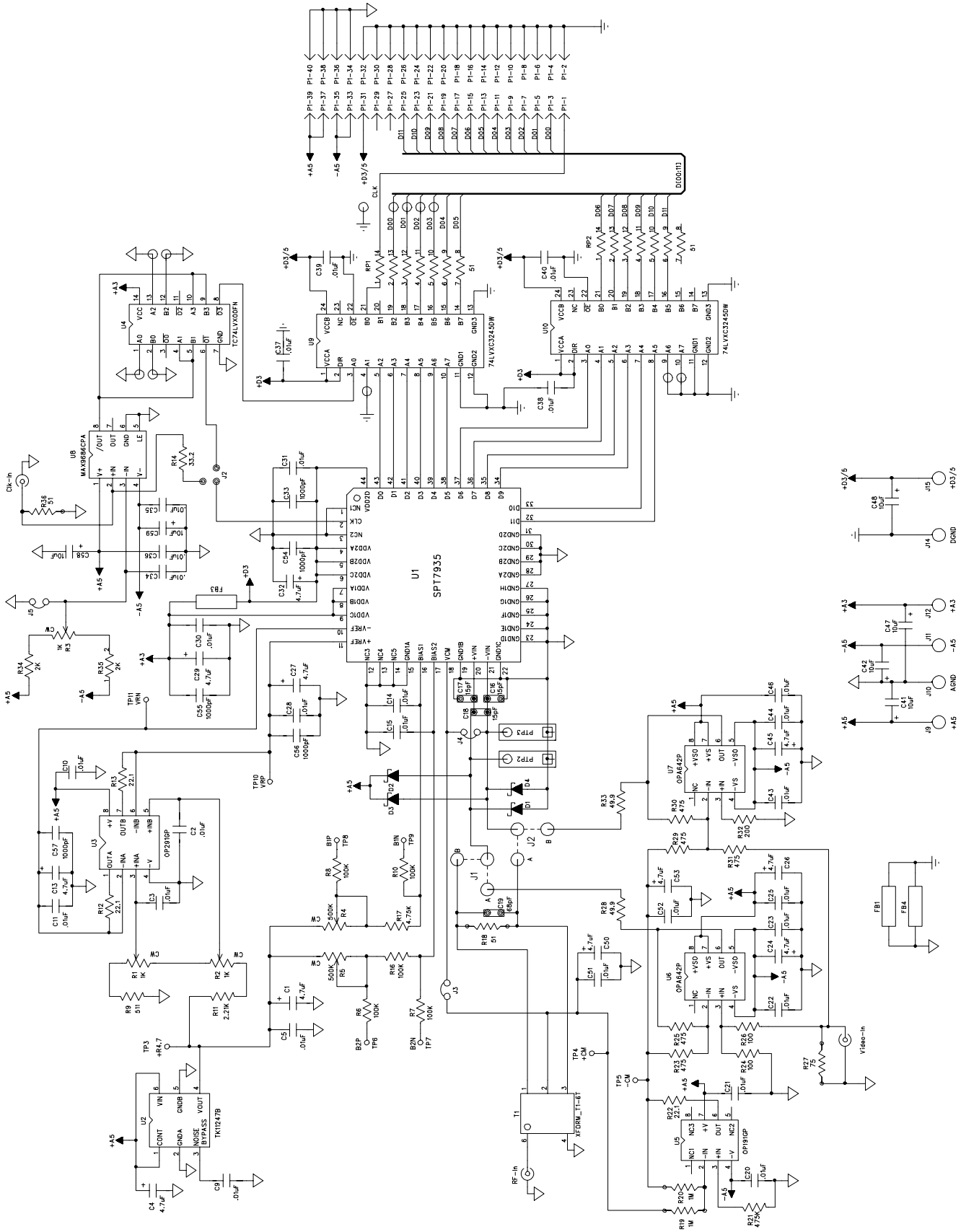


Table III - Bill of Materials

No.	Reference	Part Number	Description	Qty	Manufacturer
1	C1,4,13,24,26,27, 29,32,45,50,53	ECS-T1CY475R	4.7 µF Tantalum Chip Cap	11	Panasonic/Any
2	C2,3,5,9-11,14,15 20-23,25,28,30,31 34-40,43,44,46,51,52	ECU-V1H103KBM	.01 µF Chip Cap	28	Panasonic/Any
3	C16-18	ECU-S2A150JCA	15 pF Radial Cap (Socketed)	3	Panasonic/Any
4	C19	ECU-S2A680JCA	68 pF Radial Cap (Socketed)	1	Panasonic/Any
5	C33,54-57	ECU-V1H102KBM	1000 pF Chip Cap	5	Panasonic/Any
6	C41,42,47,48	ECS-T1CX106R	10 µF Tantalum Chip Cap	4	Panasonic/Any
7	C58,59	ECS-T1CX106R	10 µF Tantalum Chip Cap	2	Panasonic/Any
8	D1-4	SD101B	Schottky Diode	4	Liteon/Any
9	FB1,3,4	EXC-ELSA35	Ferrite Bead	3	Panasonic
10	J3-5	PZC36SAAN	Jumper, 2 Pin (Trim from 36-pin)	3	Sullins
11	J1,7,8	31-5329	Board Mount BNC	3	Amphenol
12	J9-12,14,15	108-0740-001	Banana Jack	6	Johnson
13	P1	PZC36DBAN	72 Pin Horiz Male Conn (Trim to 40-Pin)	1	Sullins
14	R1-3	3266W-1-102	1 kΩ Variable Resistor (Pot)	3	Bourns
15	R4,5	3266W-1-504	500 kΩ Variable Resistor (Pot)	2	Bourns
16	R6-8,10,16	ERJ-8ENF1003	100 kΩ 1/8 W 1% Chip Resistor	5	Panasonic/Any
17	R9	ERJ-8ENF5110	511 Ohm 1/8 W 1% Chip Resistor	1	Panasonic/Any
18	R11	ERJ-8ENF2211	2.21 kΩ 1/8 W 1% Chip Resistor	1	Panasonic/Any
19	R12,13,22	ERJ-8ENF22R1	22.1 Ohm 1/8 W 1% Chip Resistor	3	Panasonic/Any
20	R14	ERJ-8ENF33R2	33.2 Ohm 1/8 W 1% Chip Resistor	1	Panasonic/Any
21	R17	ERJ-8ENF4751	4.75 kΩ 1/8 W 1% Chip Resistor	1	Panasonic/Any
22	R18,36	51 MF	51 Ohm 1/4 W 1% Axial Socketed)	2	Yageo/Any
23	R19,20	1.0M MF	1.0M 1/4 W 1% Axial (Socketed)	2	Yageo/Any
24	R21	ERJ-8ENF4753	475 kΩ 1/8 W 1% Chip Resistor	1	Panasonic/Any
25	R23,25,29-31	ERJ-8ENF4750	475 Ohm 1/8 W 1% Chip Resistor	5	Panasonic/Any
26	R24,26	ERJ-8ENF1000	100 Ohm 1/8 W 1% Chip Resistor	2	Panasonic/Any
27	R27	75 MF	75 Ohm 1/4 W 1% Axial (Socketed)	1	Yageo/Any
28	R28,33	ERJ08ENF49R9	49.9 Ohm 1/8 W 1% Chip Resistor	2	Panasonic/Any
29	R32	ERJ-8ENF2000	200 Ohm 1/8 W 1% Chip Resistor	1	Panasonic/Any
30	R34,35	ERJ-8ENF2001	2.0 kΩ 1/8 W 1% Chip Resistor	2	Panasonic/Any
31	RP3-4	760-3-R51	51 Ohm 7-Res DIP Array	2	CTS/Any
32	T1	T1-6T (KK81)	RF Transformer	1	Mini-Circuits
33	TP1,3-12,14,16-19	40F6045	Solder Terminal	16	Newark
34	U1	SPT7935	12-Bit 20 MSPS ADC	1	Fairchild
35	U2	TK11247B	Volt Regulator With On/Off	1	Toko
36	U3	OP291GP	Dual R-R Op Amp	1	Analog Devices
37	U4	TC74LVX00FN	Low Volt Quad NAND Gate	1	Toshiba
38	U5	OP191GP	R-R Op Amp	1	Analog Devices
39	U6,7	OPA642P	Low Distortion Op Amp	2	Burr-Brown
40	U8	MAX9686CPA	Fast TTL Output Comparator	1	Maxim
41	U9,10	74LVXC3245DW	Octal Bus Transceiver	2	Texas Instruments
42	N/A	1902EK-ND (Note 1)	1" Nylon Spacer	4	Digi-Key
43	N/A	H143-ND (Note 1)	4-40 Pan-Head Screw	4	Digi-Key
44	N/A	ED5044-ND	Pin Receptacle (For socketed parts)	18	Digi-Key
45	N/A	929955-06	Shunt for Jumper	3	3M (Digi-Key)
46	EB7935	Rev B	Evaluation Board	1	SAS Circuits

Note 1: Mount in four corners as bottom side legs.

Figure 7 - Component Side

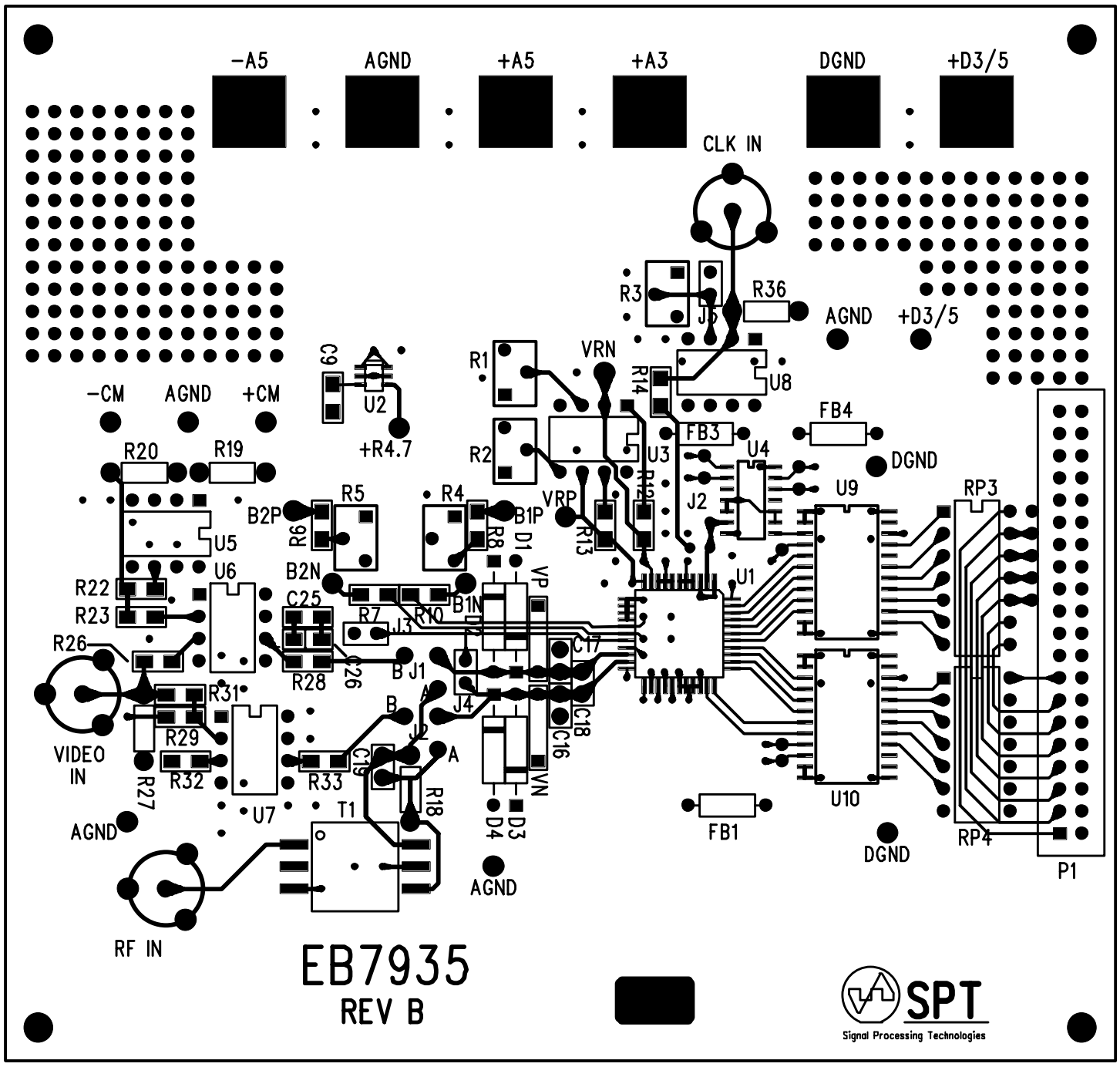


Figure 8 - Ground Layer

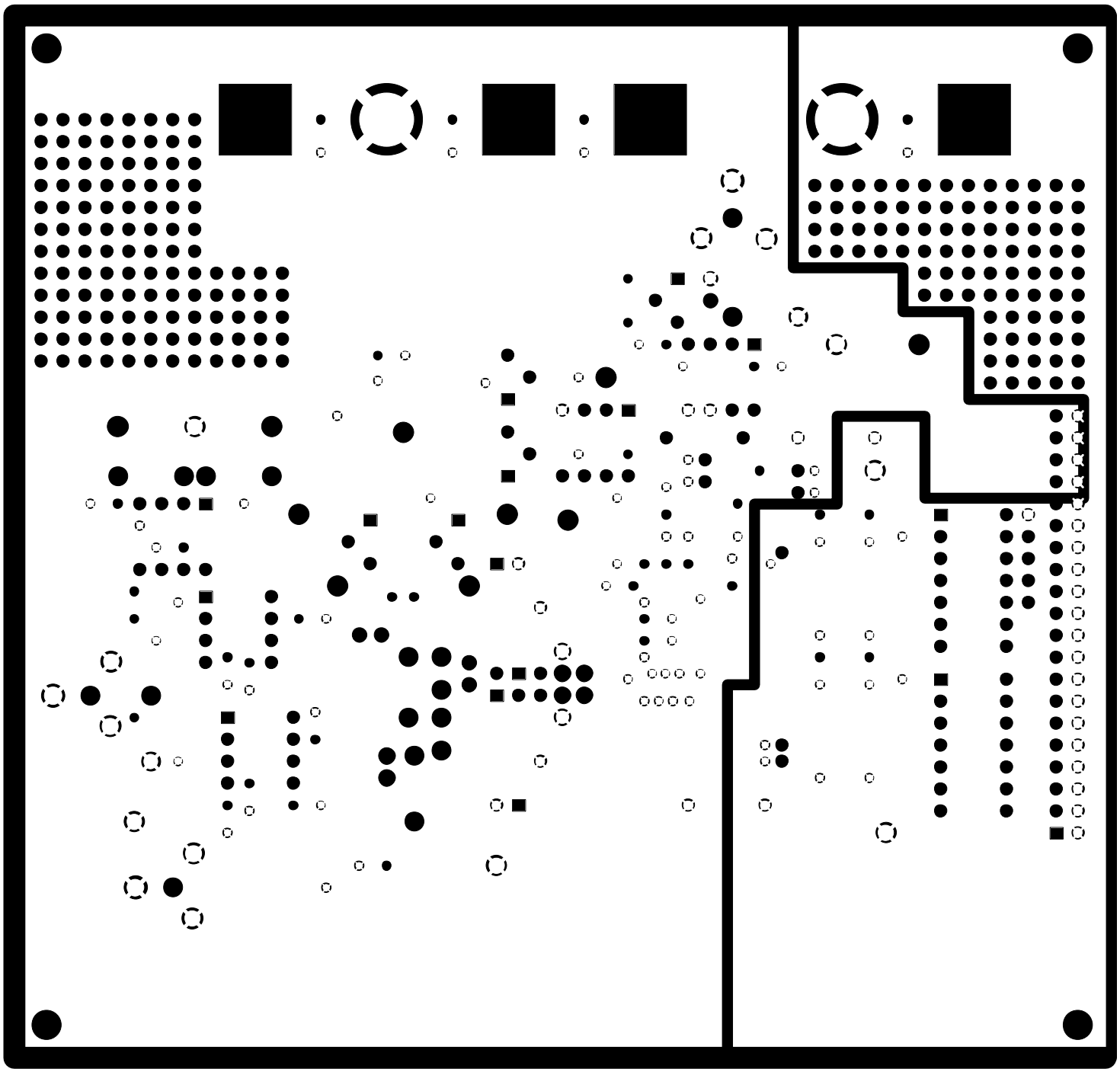


Figure 9 - Power Layer

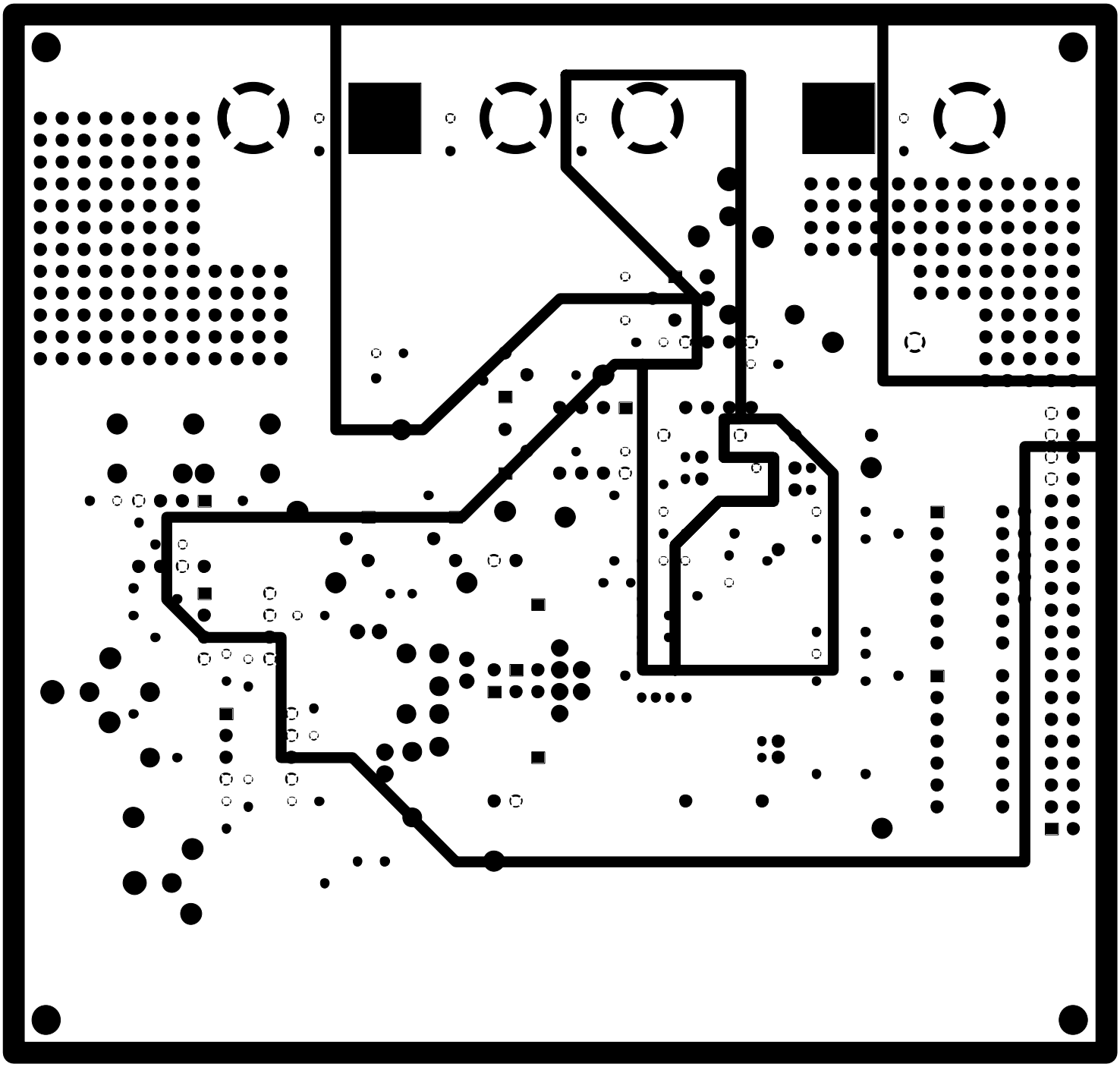
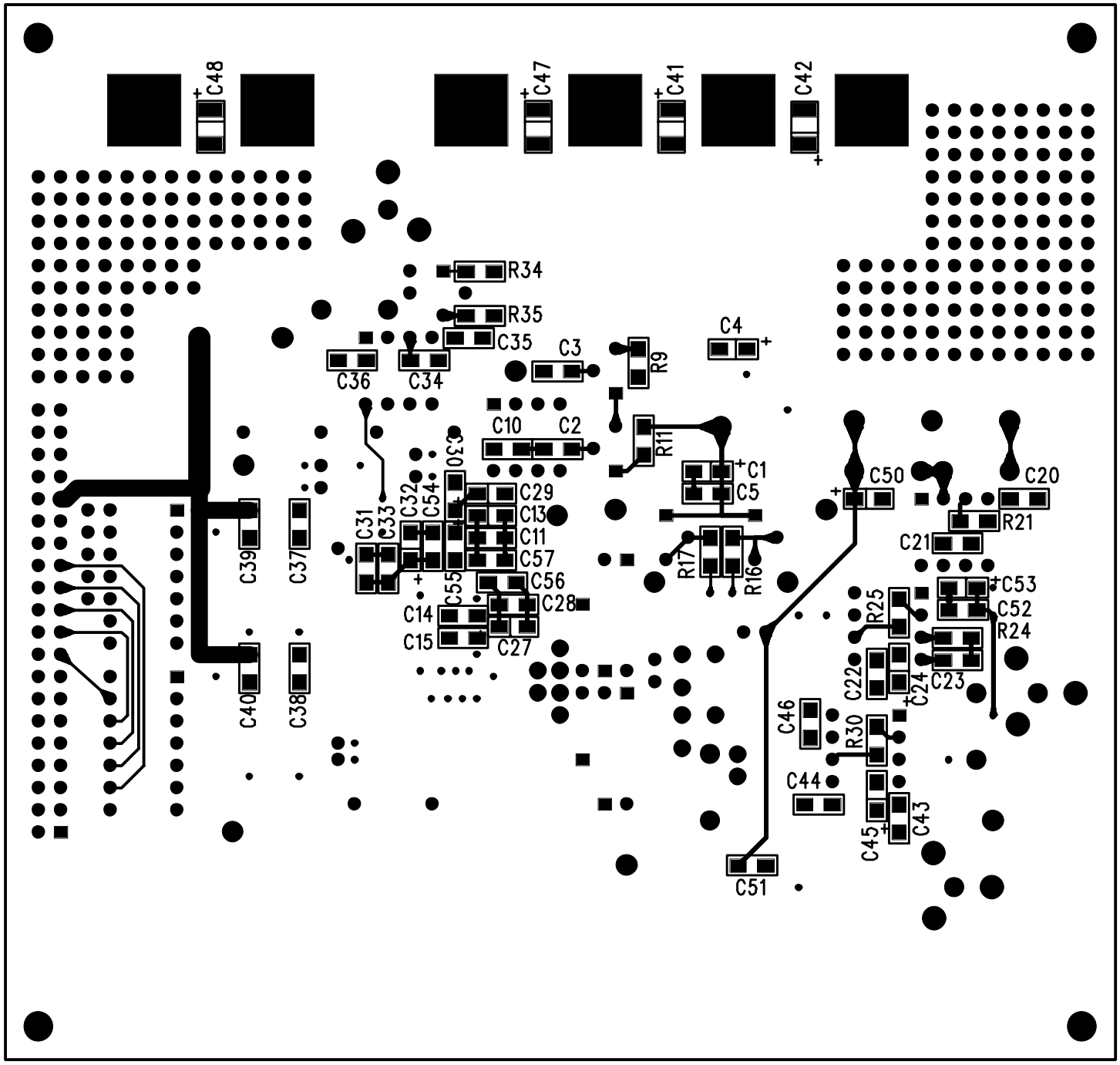


Figure 10 - Solder Side



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